What is claimed is:

1. An electronic device, comprising

    a. a substrate, having a top surface and a bottom surface;

    b. a buried layer near the top surface, electrically communicable to a drain terminal;

    c. a body region, having a second top surface, a second bottom surface and a second side surface, a portion of the side surface contacting a gate region communicable to a gate terminal;

    d. a channel region, having a third top surface, a third bottom surface, and a third side surface, the third side surface contacting the body region, the third bottom surface being substantially coplanar to the second bottom surfaces and contacting the buried layer, the third top surface being substantially coplanar to the second top surface and electrically communicable to a source region; and

    e. the source region, projecting upward from the channel region, electrically communicable to a source terminal.

2. The electronic device in claim 1 in which the substrate is a semiconductor material.

3. The electronic device in claim 2 in which the semiconductor material is p-type silicon.

4. The electronic device in claim 1 in which the buried layer is n-type silicon material communicable to a drain terminal near the top surface through a sinker.

5. The electronic device in claim 1 in which the body region comprises two layers of substantially mono-crystalline p-type silicon layers.

6. The electronic device in claim 1 in which a portion of the body region contacts a dielectric region.

7. The electronic device in claim 6 in which the dielectric region comprises a silicon dioxide region formed with a STI technique.

8. The electronic device in claim 1 in which the channel region comprises of three groups of n-type dopant ions distributed along a direction perpendicular to the top surface of the substrate.

9. The electronic device in claim 1 in which the dopant ion distribution in the channel region is lighter near the source region than near the drain region.

10. The electronic device in claim 1 in which the gate region is substantially p-type polycrystalline silicon.

11. The electronic device in claim 1, in which an electrical current flows in the channel region upon a voltage bias being applied between the source terminal and the drain terminal.

12. The electronic device in claim 11, in which the electrical current flows in a direction substantially perpendicular the top surface of the substrate.

13. The electronic device in claim 11, in which the magnitude of the current is a function of a voltage at the gate terminal.

14. The electronic device in claim 1, in which the channel region is doped with n-type dopant.

15. The electronic device in claim 1, in which the channel region is doped with p-type dopant.

16. A semiconductor integrated circuit device, comprising

a. a semiconductor substrate, having a top surface and a bottom surface;

b. a buried layer of crystalline semiconductor material near the top surface, doped with a dopant of a first polarity, electrically communicable to a drain terminal near the top surface;

c. a mono-crystalline first region, doped with dopant of the first polarity, having a top surface, a bottom surface and a side surface, the lower portion of the side surface contacting an electrically insulating region and the upper portion of the side surface coupling to a gate region communicable to a gate terminal near the top surface of the substrate;

d. a channel region, doped with dopant of a second polarity, having a top surface, a bottom surface, and a side surface, the top surface being substantially coplanar to the top surface of the first region, the bottom surface being substantially coplanar to the bottom surfaces of the first region and electrically communicable to the buried layer, the side surface contacting the first region; and

e. a source region, projecting upward from the channel region, having a top surface electrically communicable to a source terminal, a bottom surface electrically communicable to the top surface of the channel region.

17. The electronic device in claim 16, in which an electrical current flows in the channel region upon a voltage bias being applied between the source terminal and the drain terminal.

18. The electronic device in claim 17, in which the electrical current flows in a direction substantially perpendicular the top surface of the substrate.

19. The electronic device in claim 17, in which the magnitude of the current is a function of a voltage at the gate terminal.

20. The electronic device in claim 16, in which the distance between the top surface and the bottom surface of the channel region is about 0.7 micro-meters, in which about 0.5 micro-meter is attributable to a bottom layer and about 0.2 micro-meters is attributable to a top layer.

21. The electronic device in claim 16, in which the dopant of a first polarity is p-type.

22. The electronic device in claim 16, in which the dopant of a first polarity is n-type.

23. An n-channel silicon JFET, comprising

a. a silicon substrate, having a top surface and a bottom surface;

b. a buried layer of mono-crystalline silicon near the top surface, doped with a n-type dopant to a sheet resistance of about 25 ohms per square, the buried layer being electrically communicable to a drain terminal near the top surface of the substrate;

c. a silicon mono-crystalline first region, doped with p-type dopant to a concentration of about $1x10^{15}$ dopant ions per cubic centimeter, having a top surface, a bottom surface and a side surface, the distance between the top and the bottom surfaces being about 0.7 micrometers, the lower portion of the side surface being in contact with a silicon dioxide region and the upper portion of the side surface being in contact with a p-type, poly-crystalline silicon gate region;

d. the silicon gate region being communicable to a gate terminal near the top surface of the substrate;

e. an n-type silicon mono-crystalline-channel region, doped with n-type dopant to a concentration higher than about $1x10^{15}$ dopant ions per cubic centimeter, having a top surface, a bottom surface, and a side surface, the top surface being substantially coplanar to the top surface of the p-type first region, the bottom surface being substantially coplanar to the bottom surfaces of the p-type region in c and electrically communicable to the buried layer, the side surface contacting the p-type first region;

f. a first n-type, poly-crystalline-silicon-source region, projecting upward from the channel region and the gate region, having a top surface electrically communicable to a source terminal near the top surface of the substrate, a bottom surface electrically communicable to the top surface of the channel region, a side surface in contact with dielectric sidewall spacers;

g. the first n-type, poly-crystalline-silicon-source region in f being electrically insulated from the first p-type, poly-crystalline-silicon-gate region.

h. the device being operable channeling an electrical current through the channel region upon a voltage bias being applied between the source terminal and the drain terminal; and

i. the electrical current flowing in a direction substantially perpendicular the top surface of the silicon substrate, the magnitude of the electrical current being a function of a voltage at the gate terminal.

24. An method for making an electronic device, comprising

a. providing a semiconductor substrate of a first conductivity, having a top surface and a bottom surface;

b. forming a buried layer of a second conductivity near the top surface;

c. forming a first semiconductor-layer over the buried layer, doping the region with dopant of the first conductivity;

d. forming in the first layer insulation regions that isolate an island of the first-layer material, the insulation regions having substantially the same thickness as the first layer so the insulation regions reaches the buried layer;

e. forming a second semiconductor-layer of the first conductivity over the first semiconductor-layer and the insulation regions, portions of the second layer over the insulation regions being polycrystalline, portions of the second layer over the first layer being mono-crystalline;

f. forming a dielectric layer over the second layer;

g. implanting dopant of the second conductivity into the island of the first semiconductor layer to form a channel-region in the first and the second semiconductor-layer that reaches the buried layer;

h. forming a third semiconductor-layer of the second conductivity over the dielectric layer;

i. patterning and etching the third semiconductor-layer and the dielectric layer to form a gate structure and uncovering a portion of the second semiconductor-layer; and

j. implanting dopant of the first conductivity into the uncovered second semiconductor-regions to form a gate structure.

25. The method in claim 24, in which the semiconductor substrate is silicon.

26. The method in claim 24, in which the insulation regions comprise silicon dioxide formed with a STI technique.

27. The method in claim 24, in which the first semiconductor layer is about 0.5 micrometers thick and the second semiconductor layer is about 0.2 micrometers thick.

28. The method in claim 24, in which the dielectric layer comprises silicon dioxide and silicon nitride.

29. The method in claim 24, in which the implanting into the first semiconductor layer comprises three implant energies and three implant dosages.

30. The method in claim 24, in which a portion of the dopant implanted into the gate structure diffuses into the mono-crystalline portion of the second semiconductor layer.

31. The method in claim 24, in which the first conductivity is p-type.

32. The method in claim 24, in which the first conductivity is n-type.

33. A method for making an n-channel silicon JFET, comprising

a. providing a p-type silicon substrate, having a top surface and a bottom surface;

b. forming a buried layer of mono-crystalline silicon near the top surface, doped with a n-type dopant to a sheet resistance of about 25 ohms per square;

c. forming a 0.5 micrometers silicon mono-crystalline first layer over the buried layer, doping the region with p-type dopant to a concentration of about $1x10^{15}$ dopant ions per cubic centimeter;

d. forming in the first layer insulation regions that isolate islands of the first-layer material, the insulation regions having substantially the same thickness as the first layer so the insulation regions contact the buried layer;

e. forming a 0.2 micrometer silicon second layer over the first layer and the insulation regions, portions of the second layer over the insulation regions being polycrystalline silicon, portions of the second layer over the first layer being mono-crystalline silicon, doping the second layer with p-type dopant to a concentration of about $1x10^{15}$ dopant ions per cubic centimeter;

f. forming a dielectric layer of silicon dioxide and silicon nitride over the second layer;

g. patterning and etching the dielectric layer to form a opening region free of the dielectric material over the second layer;

h. implanting n-type dopant through the opening region to form a n-type channel-region that reaches the buried layer;

i. forming a third n-type silicon layer over the dielectric layer;

j. patterning and etching the third silicon layer and the dielectric layer to form a source structure and uncovering a portion of the second silicon layer; and

k. implanting p-type dopant into the uncovered second-silicon regions to form a gate structure.